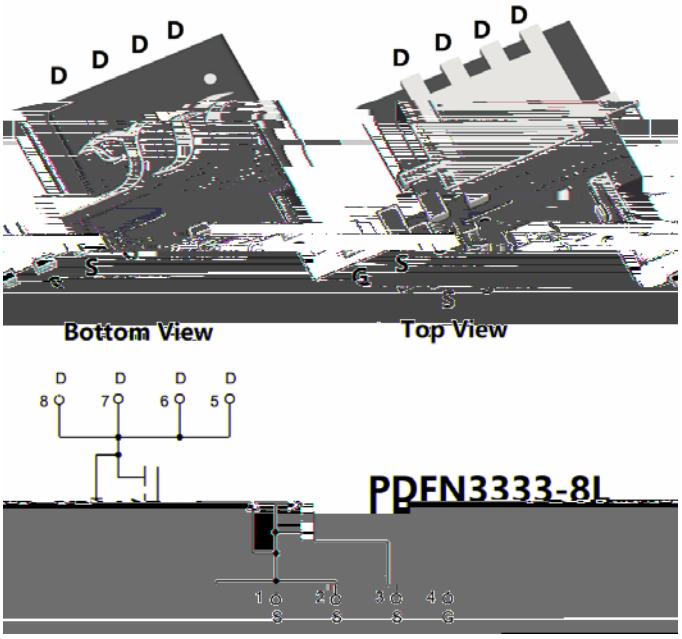
N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 40V
- I_D 50A
- $R_{DS(ON)}$(at V_{GS}=10V) 6.9mΩ
- 100% EAS Tested
- 100% V_{DS} Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor
- 12V Automotive systems

■ Absolute Maximum Ratings (T_J=25 unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-source Voltage			V_{DS}	40	V
Gate-source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25 , V_{GS}= 10V	I_D	14	A
		T_A=100 , V_{GS}= 10V		9.9	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25 , V_{GS}= 10V		50	
		T_C =100 , V_{GS}= 10V		35	
Pulsed Drain Current	T_C=25 , t_p=100μs		I_{DM}	200	A
Avalanche energy	V_G=10V, R_G=25Ω, L=0.5mH, IAS=16.5A		EAS	68	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25	P_D	2.3	W
		T_A=100		1.1	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25		50	
		T_C =100		25	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55 +175	

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{θJA}$	55	65	/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{θJC}$	2.4	3	

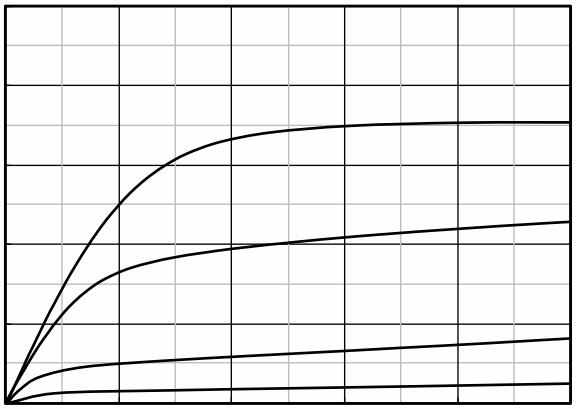
■ Ordering Information (Example)

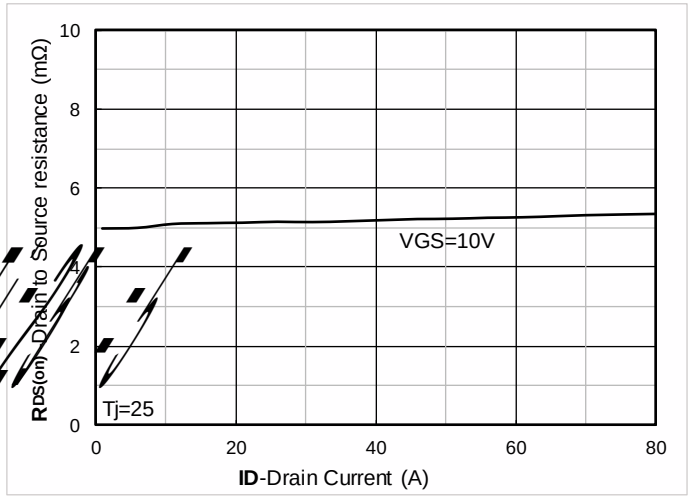
PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ6D9G04HHQ	F1	Q6D9G04	5000	10000	100000	13" reel

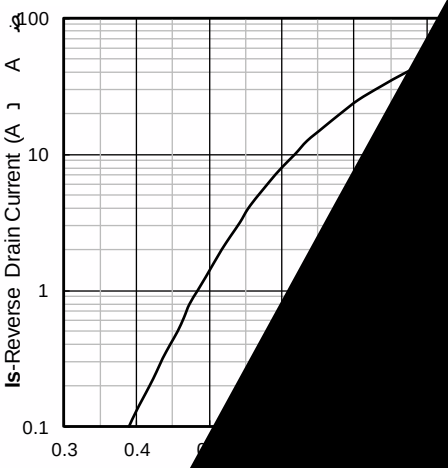
■ Electrical Characteristics (T_J=25 unless otherwise noted)

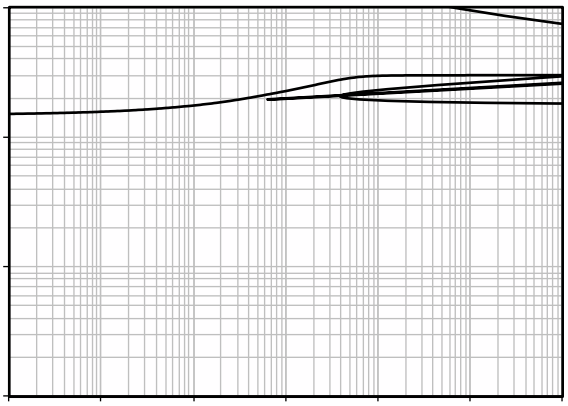
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V, V_{GS}=0V	-	-	1	μA
		V_{DS}=40V, V_{GS}=0V, Tj=125	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	2	3	4	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	5.1	6.9	mΩ
Diode Forward Voltage	V_{SD}	I_S=20A, V_{GS}				

■Typical Electrical and Thermal Characteristics Diagrams

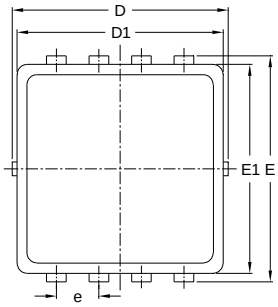



RDS(on)-Drain to Source resistance (mΩ)
10
8
6
4
2
0
VGS=10V
Tj=25
0
20
40
60
80
ID-Drain Current (A)

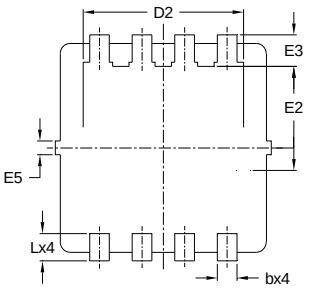

Is-Reverse Drain Current (A)
100
10
1
0.1
0.3
0.4



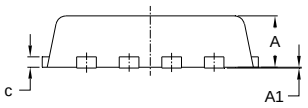
■ PDFN3333-8L-B-0.75MM Package information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

UNIT mm

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

SUGGESTED SOLDER PAD LAYOUT

'LVFODLPHU

7KH LQIRUPDWLRQ SUHVHQWHG LQ WK\LV [illegible] (O[illegible] ULJKW WR PDNH FKDQ[illegible] RIGLWV SOD\HG KHUHLQ [illegible] RWKHUZLVH

7KH SURGXFW OLVW[illegible] OLIH VDYLQJ OLIHVXV[illegible] RUOD[illegible] VXFK LPSURSHU XVH RI VDOH

7KLV SXEOLFDWLRQ [illegible] ZZZ \