P-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	-100V
I_D	-8A
$R_{DS(ON)}$(at V_{GS}=-10V)	200m
$R_{DS(ON)}$(at V_{GS}=-4.5V)	235m

100% EAS Tested

100% V_{DS} Tested

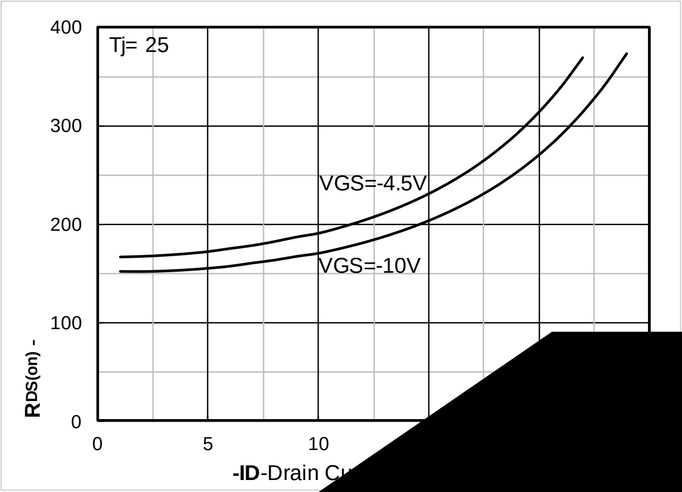
General Description

Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units

S

Typical Electrical 50.57WBT/F5 10.56Tf1 0 0 1 2.94 20.4Tm0 g0 G[2)]T4c[ica



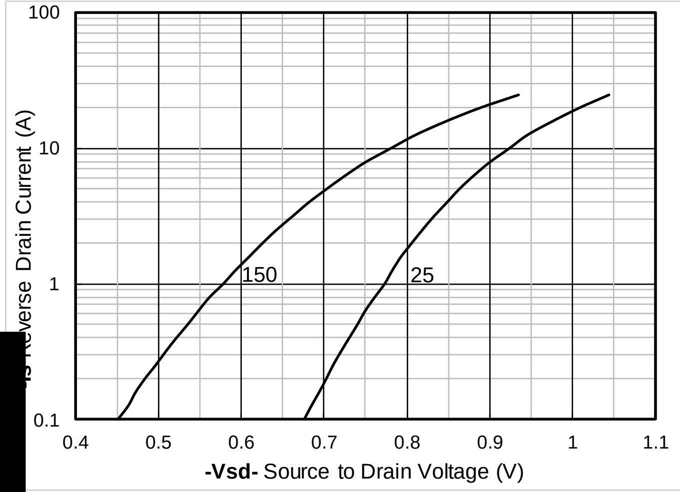


Figure 7. [redacted]

Figure [redacted]

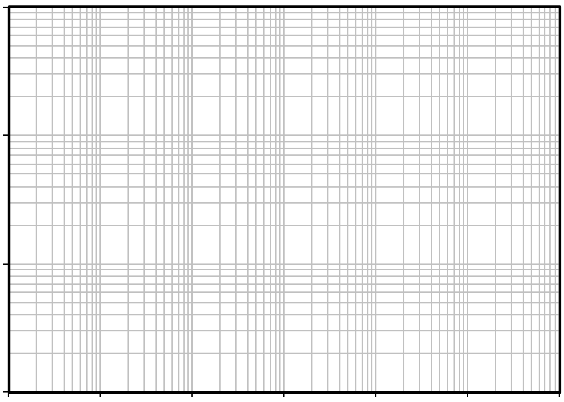


Figure 13. Maximum Transient Thermal Impedance

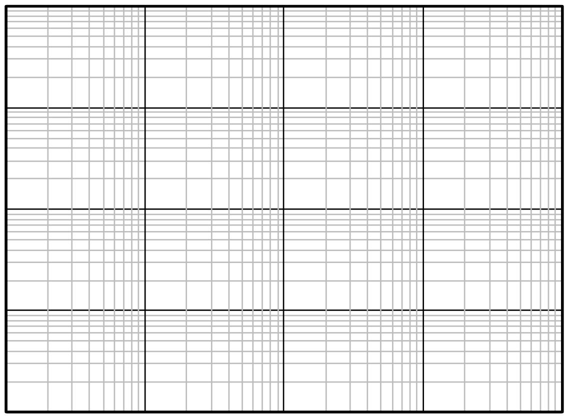
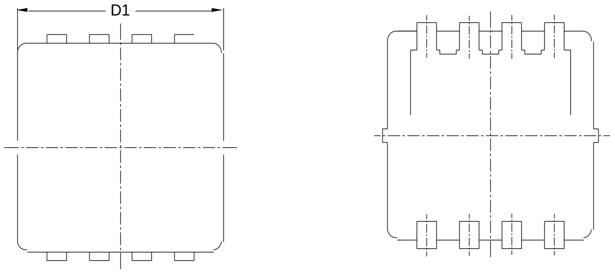


Figure 14. Safe Operation Area

PDFN3333-8L-B-0.75MM Package information



UNIT mm

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

Disclaimer

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