

## P-Channel Enhancement Mode Field Effect Transistor

### Product Summary

$V_{DS}$	-20 V
$I_D$	-115 A
$R_{DS(ON)}$ ( at $V_{GS}=-10V$ )	3.2 m
$R_{DS(ON)}$ ( at $V_{GS}=-4.5V$ )	4.0 m
$R_{DS(ON)}$ ( at $V_{GS}=-2.5V$ )	5.0 m
100% EAS Tested	
100% $V_{DS}$ Tested	

### General Description

Trench Power LV MOSFET technology  
Low  $R_{DS(on)}$  & FOM  
Extremely low switching loss  
Excellent stability and uniformity  
High density cell design for low  $R_{DS(ON)}$   
Moisture Sensitivity Level 1  
Epoxy Meets UL 94 V-0 Flammability Rating  
Halogen Free



# YJG115P02A

## Typical Electrical and Thermal Characteristics Diagrams

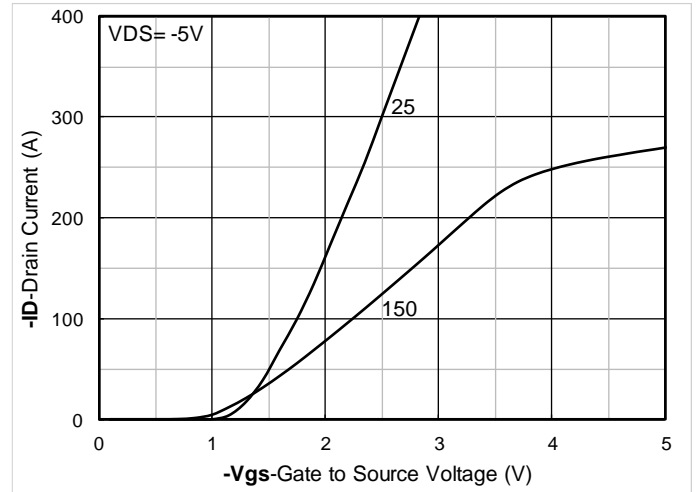
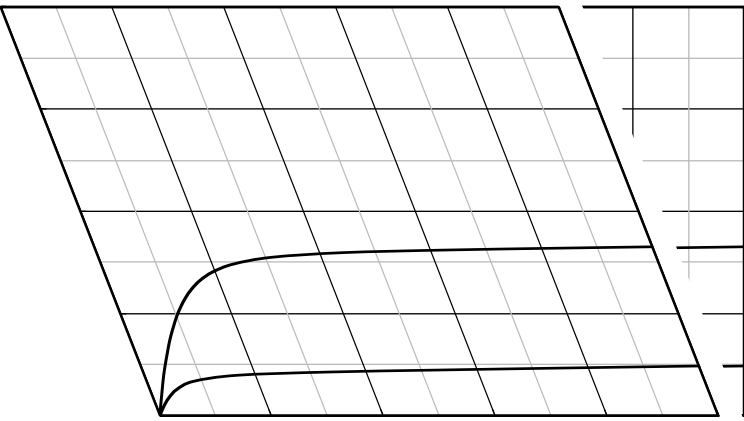


Figure 1.



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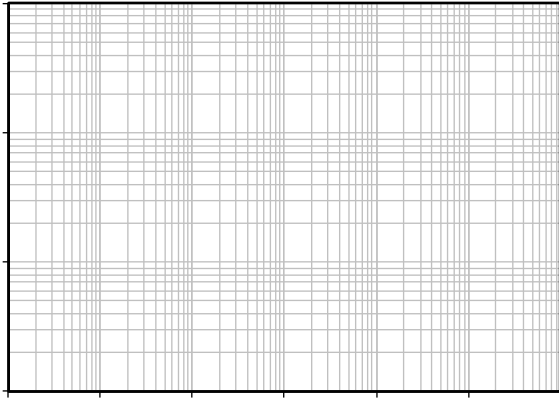


Figure 13. Maximum Transient Thermal Impedance

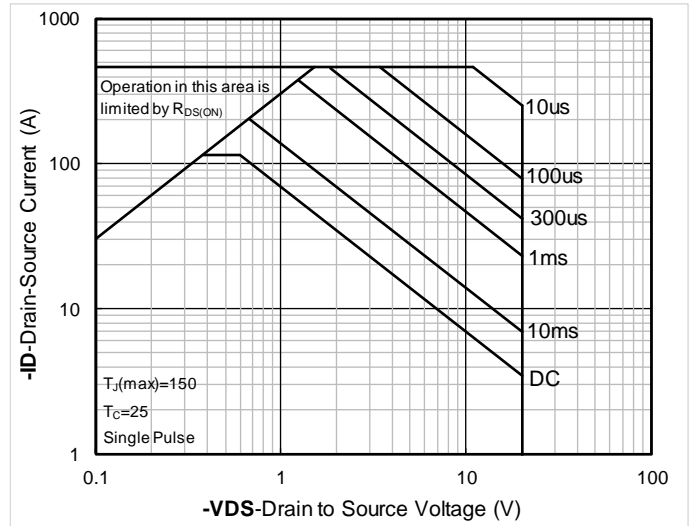
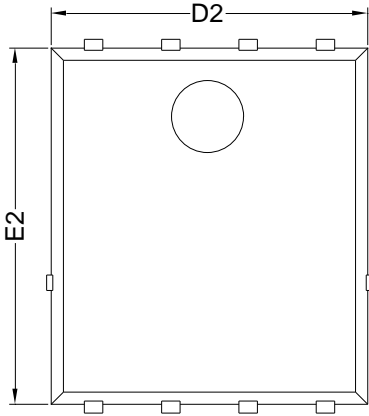


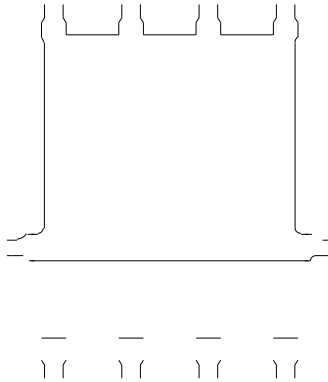
Figure 14. Safe Operation Area

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## PDFN5060-8L-B-1.1MM Package information



Top View



Bottom View

Side View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

**Note:**

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10$ mm.
3. The pad layout is for reference purposes only.

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