

# YJD08C65HJ

## N-Channel Enhancement Mode Field Effect Transistor

### Product Summary

$V_{DS}$	650V
$I_D$	8A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	580m
100% EAS Tested	
100% $V_{DS}$ Tested	

### General Description

YJD08C65HJ is a N-channel enhancement mode MOSFET, with a maximum drain current of 8A and a maximum drain-source voltage of 650V. It is suitable for use in power switching applications.

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## Electrical Characteristics (T<sub>J</sub>=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub>	650	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =650V, V <sub>GS</sub> =0V	-	-	1	
		V <sub>DS</sub> =650V, V <sub>GS</sub> =0V, T <sub>J</sub> =150	-	-	100	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±30V, V <sub>DS</sub> =0V	-	-	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub>	2.8	3.3	3.8	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =4A	-	530	580	m
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =8A, V <sub>GS</sub> =0V	-	-	1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>		-	-	8	A
<b>Dynamic Parameters</b>						
Capacitance	C <sub>iss</sub>		-	465	-	
		V <sub>DS</sub> =325V, V <sub>GS</sub> =0V, f=1MHz				pF

# YJD08C65HJ

## Typical Electrical and Thermal Characteristics Diagrams

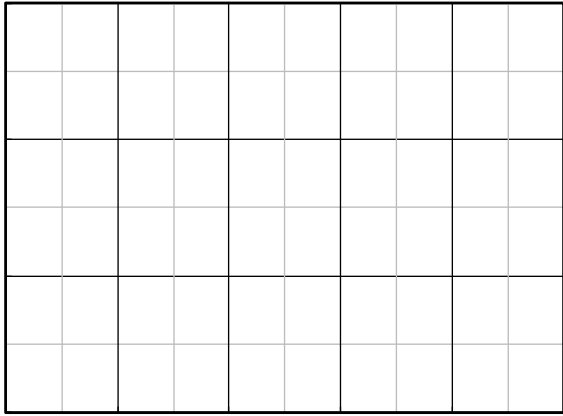


Figure 1. Output Characteristics

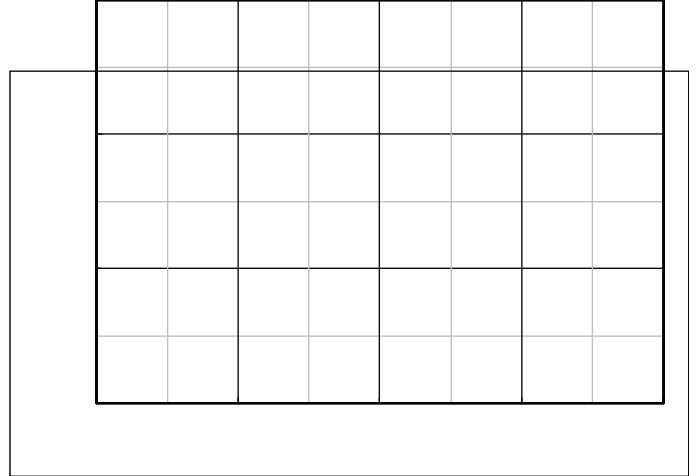


Figure 2. Transfer Characteristics

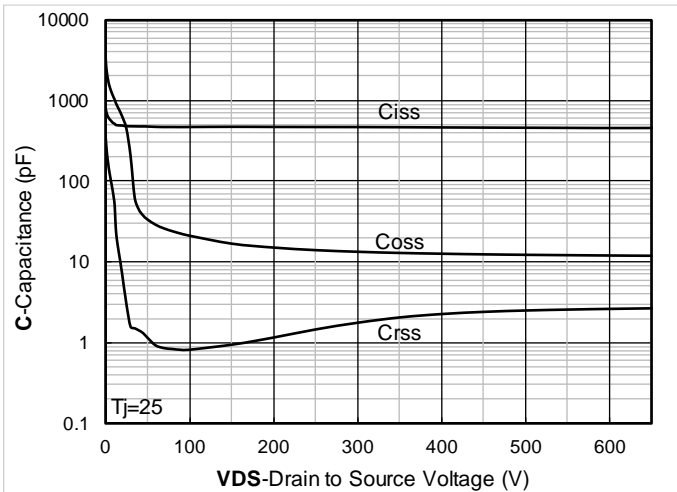


Figure 3. Capacitance Characteristics

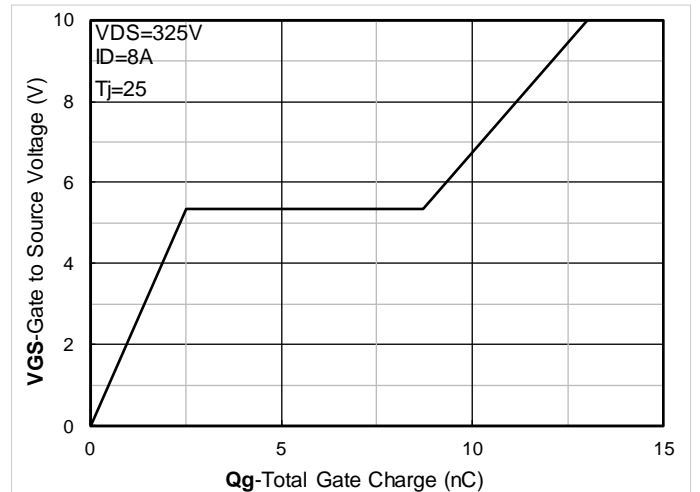


Figure 4. Gate Charge

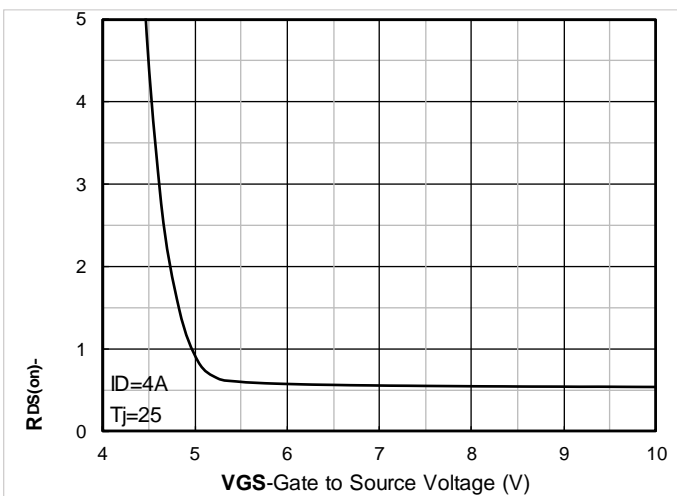


Figure 5. On-Resistance vs Gate to Source Voltage

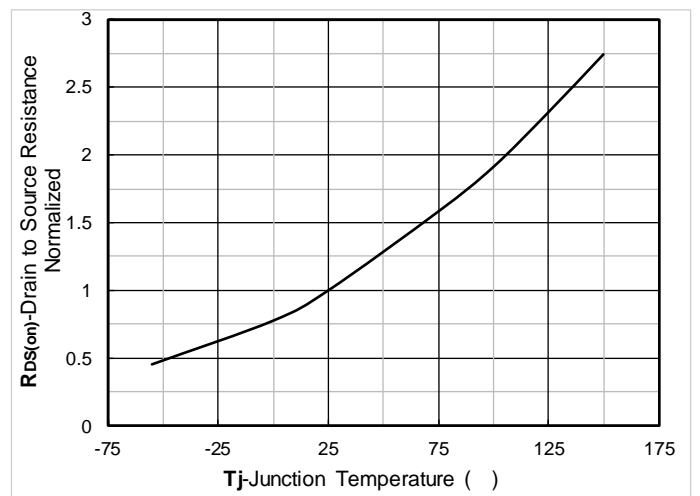


Figure 6. Normalized On-Resistance

# YJD08C65HJ

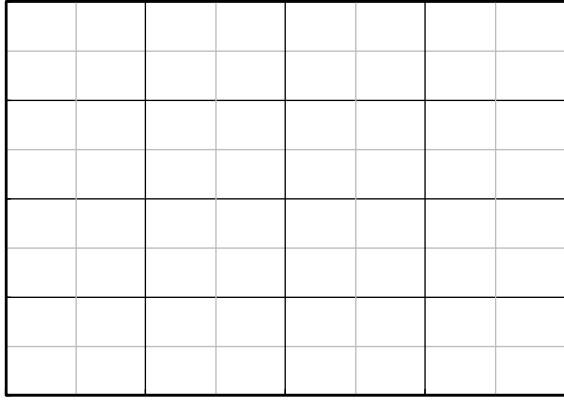


Figure 7.  $R_{DS(on)}$  VS Drain Current

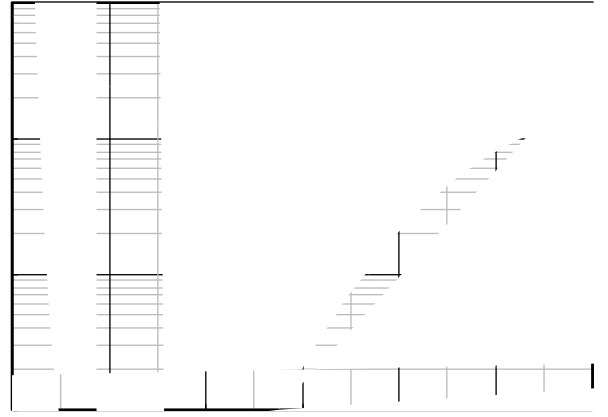


Figure 8. Forward characteristics of reverse diode

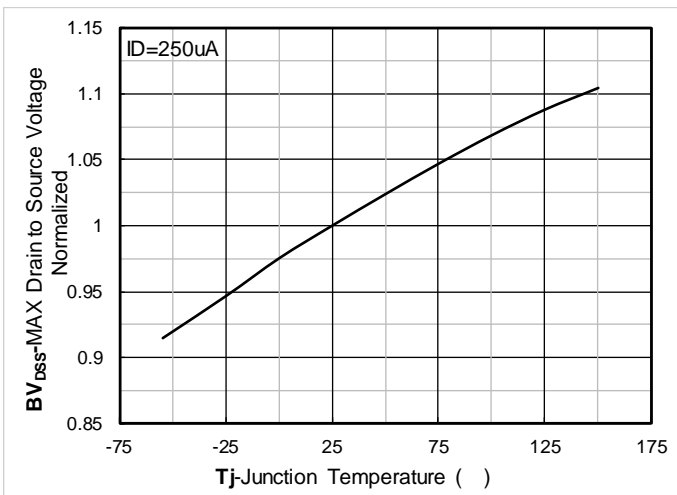


Figure 9. Normalized breakdown voltage

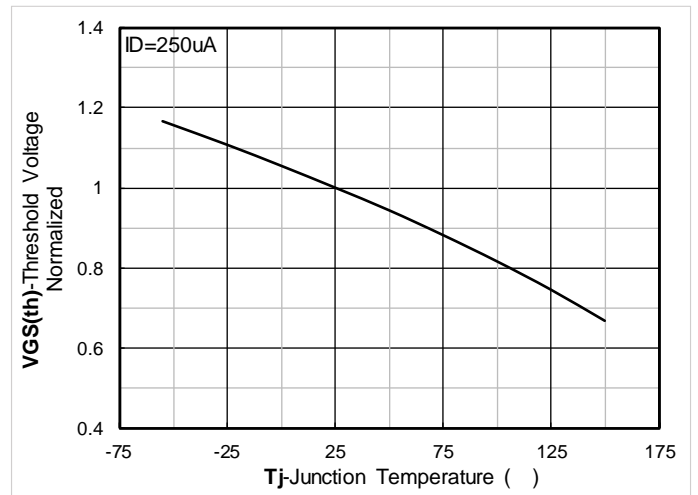


Figure 10. Normalized Threshold voltage

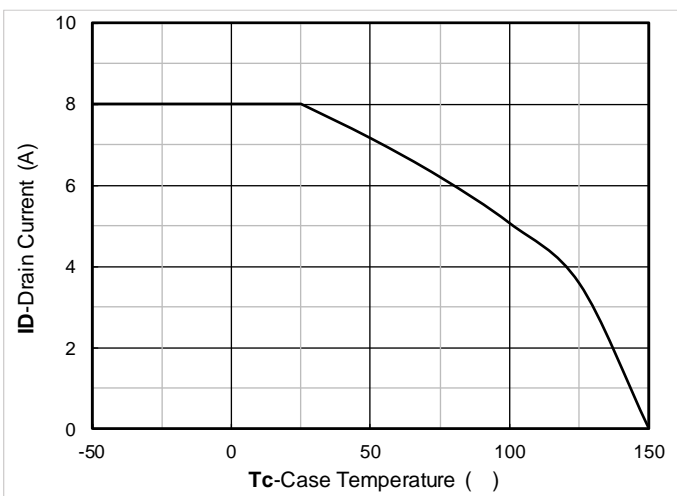


Figure 11. Current dissipation

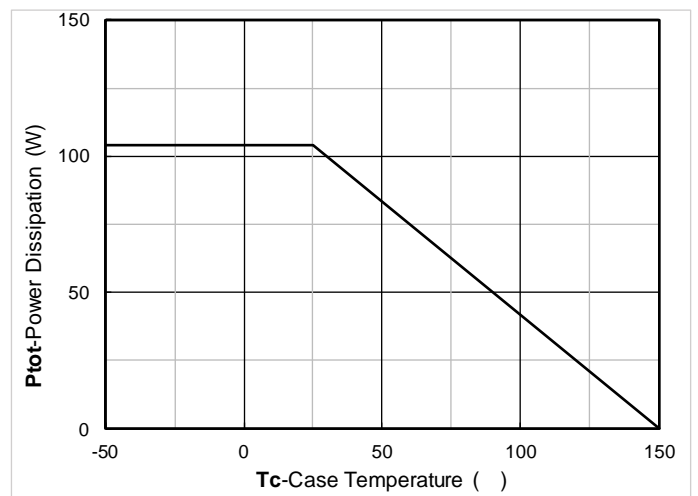


Figure 12. Power dissipation

# YJD08C65HJ

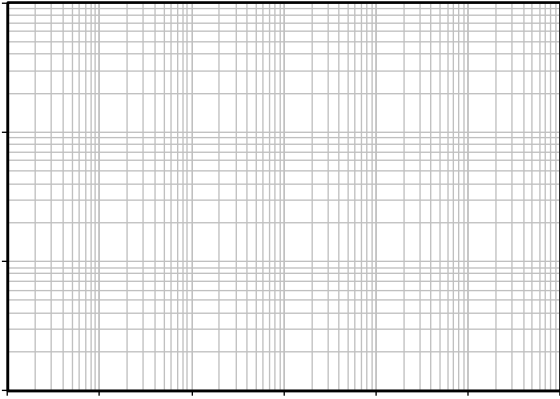


Figure 13. Maximum Transient Thermal Impedance

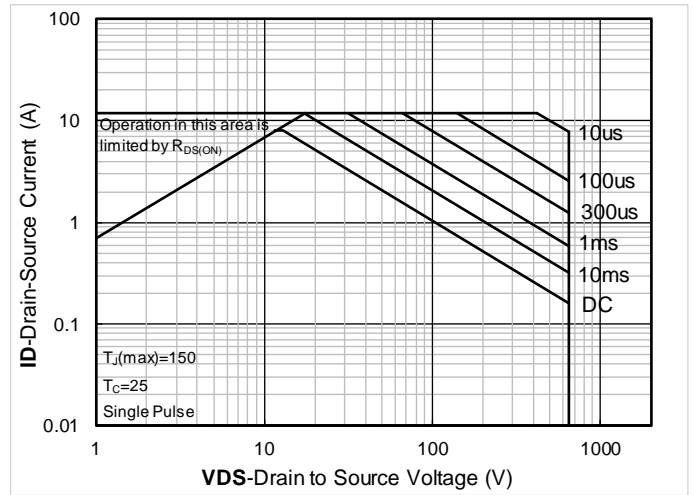


Figure 14. Safe Operation Area

## Test Circuits

# YJD08C65HJ

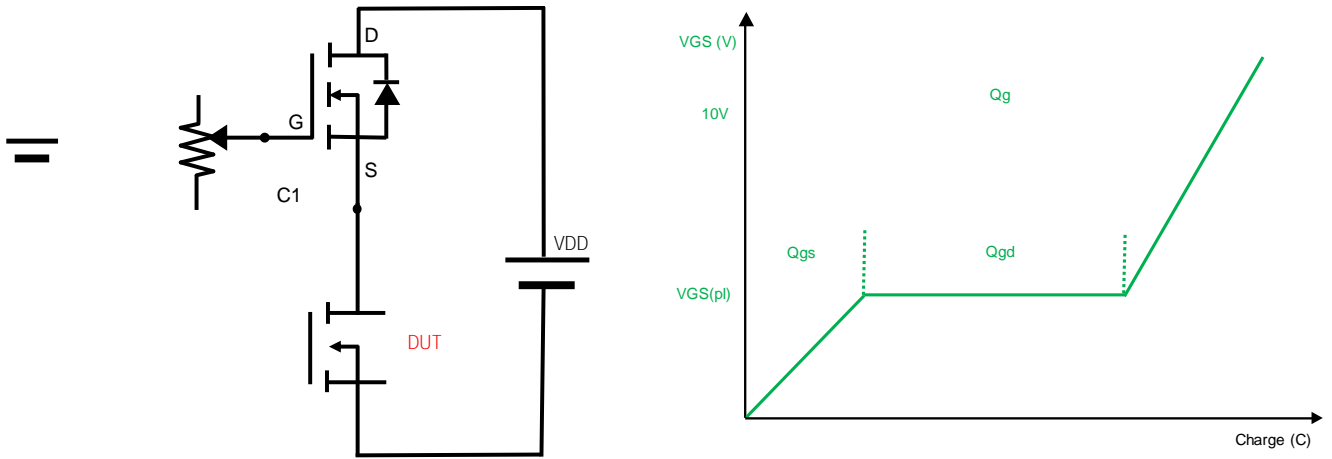


Figure B. Gate Charge Test Circuit & Waveform

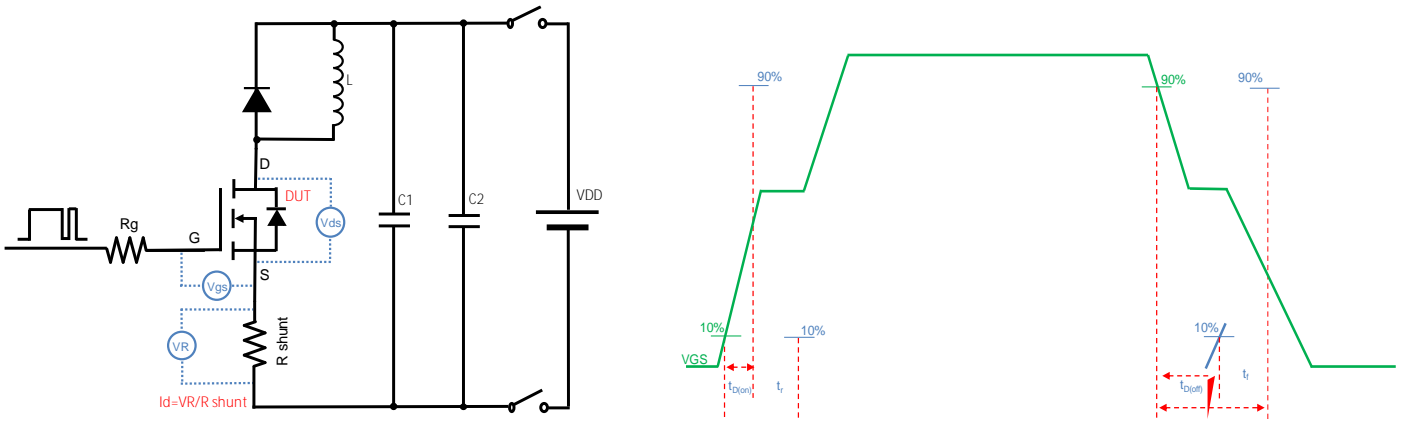


Figure C. Resistive Switching Test Circuit & Waveform

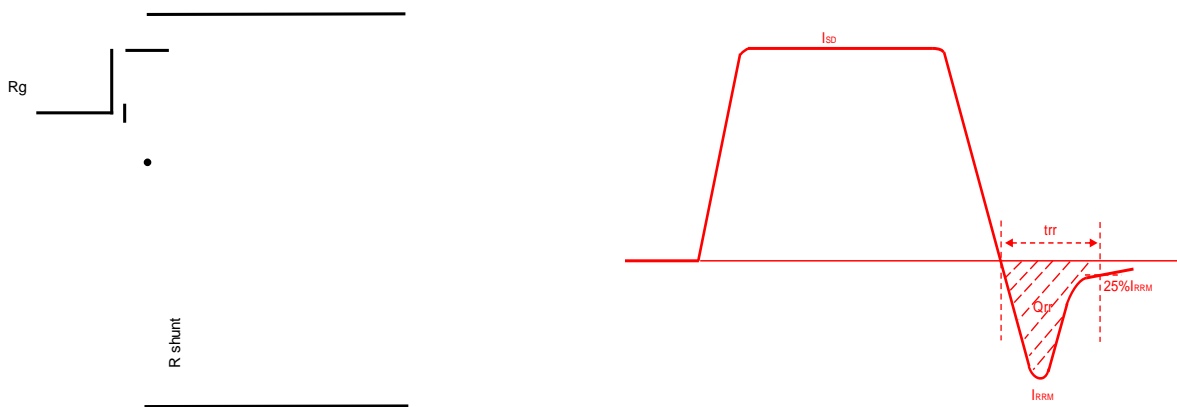


Figure D. Diode Recovery Test Circuit & Waveform



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## Disclaimer

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